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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,122	02/02/2004	Fabio Campi	61181-00012USPX	7254
7590	03/23/2006			EXAMINER
Andre M. Szuwalski JENKENS & GILCHRIST, A PROFESSIONAL CORPORATION Suite 3200 1445 Ross Avenue Dallas, TX 75202			COLEMAN, ERIC	
			ART UNIT	PAPER NUMBER
			2183	
DATE MAILED: 03/23/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/770,122	CAMPET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-25 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye (patent No. 6,518,965) in view of Yano (patent No. 6,901,502) and DeHon (patent No. 6,052,773).

3. Dye taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 1,):

Embedded processor (embedded RISC)(e.g., see fig. 2b) including a microcontroller and memory device comprising a processor (140) (integrated memory controller) structured to implement a Very Long Instruction Word elaboration mode by a hardwired computational logic (processor comprises a VLIW-RISC engine e.g., see col. 17, lines 62-67) and an additional elaboration channel (channel to element 172,144,174) (or elements 235 or 23). Dye did not expressly detail the function unit was reconfigurable. Yano however taught a embedded FPGA (19)on the same semiconductor as the CPU (e.g., see fig. 1) a reconfigurable function unit based on a pipelined array or configurable lookup based cells (e.g., see fig. 12) controlled by a special purpose control unit (17)(e.g., see fig. 1). Yano and Dye did not expressly detail

that the cell were lookup based cells. DeHon however taught a on chip configurable array comprising lookup based cells (e.g. see fig. 2,2f,5).

4. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dye and Yano. Both references were directed toward the processing of data using signal processing units. One of ordinary skill would have been motivated to add the Yano teachings of reconfiguring the FPGA at least to provide a system that could adapt to differing applications.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dye and Dehon. . Both references were directed toward the processing of data using signal processing units. One of ordinary skill in the DP art would have been motivated to incorporating the lookup cells teaching Dehon to facilitate programming of the array.

6. As to limitations of claim 2,3,9 Yano taught the reconfigurable function unit includes a hardware based Field Programmable Gate array embedded device tightly integrated in the processor core receiving input from a dedicated channels to/from the CPU. file(e.g., see fig. 1). Since it was well known in the for the CPU to utilize registers to store input and output such as results. It would have obvious to one of ordinary skill that the data sent from the FPGA to or from the CPU would have been stored in registers for use by the CPU. On the other hand DeHon taught transfer to/from registers (e.g., see figs. 2, 2d, 2f). As to the control unit being Data-flow-graph based, the cited references operate the data is present in a synchronous manner (e.g., see fig. 1e of DeHon) therefore the references teach the limitation to the extent claimed.

7. As to claim 4, claims as the claim is understood Yano taught the limitation where the Yano system provided for configuration of the system at runtime (e.g., see fig. 1) a configurable lookup table based cells (e.g. see fig. 12) and variable latency data path [at least the latency for transmission receipt of data would have depended on the amount of traffic and the bandwidth of the data path where the amount of traffic would vary]. On the other hand DeHon taught a multiple latency data path (e.g., see col. 7, line 63-col. 8, line 52).

8. As to claim 5, Yano taught an architecture based on at least three flows of data between elements (e.g., see figs. 1,11 that can occur concurrently two of which feed by instruction fetch(to diagnosing portion and to configuration data tag element 22) (e.g. see fig. 1) and at least one variable latency pipeline implemented on the configurable data path from configuration memory to FPGA 19 in figure 1).

9. As to claim 6, Yano taught an FPGA is configured to perform operations that could be performed by the CPU and therefore virtually emulates a microprocessor data path (e.g., see col. 12, lines 1-57).

10. As to claim 7, Dehon (e.g., see fig. 5) taught the grouping of the cells into rows.

11. As to each representing a stage of a pipeline, since in processing in an array would at times be from one row at time that flow from one row to a succeeding row from then the rows represent a possible state of a customized pipeline or a whole array can be represented by a control data flow graph each group or rows corresponding to a different store.

12. As to claims 8,10The locking or of a register to prevent a data hazard was well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated in the implementation of the Dye, Yano and DeHon teaching to lock a register when there was a data conflict with a another instruction that required access to the register. Therefore since the data would not have been accessed then the system would have had to stall processing in the pipeline that was locked out until the data for the competing operation was completed and written back. Clearly this supports highest possible level of resource utilization as it support concurrent execution of instructions as was well known in the art at the time of the claimed invention.

13. As to claims 11,13 the DeHon taught a register file and one of ordinary skill would have been motivated to provide as many read and write ports as possible to allow for the simultaneous access to data for processing and to provide for the widest possible bus so that the widest data could be transmitted at one time. The provision of four read ports and two write ports and 32 and 64 bit buses were within the level skill of one of ordinary skill in the art at the time of the claimed invention.

14. As per claim 12, Yano taught cache means (11) or storing configuration for the logic cells (e.g., se fig. 1).

15. As per claim 14, Dehon taught configuration at the same time as execution (e.g. see col. 21, lines 1-13)

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 15,16,20,21 are rejected under 35 U.S.C. 102(e) as being anticipated by Dye.

17. Dye taught the invention as claimed including a data processing system comprising: Embedded processor (embedded RISC)(e.g., see fig. 2b) including a microcontroller and memory device comprising a processor (140) (integrated memory controller) structured to implement a Very Long Instruction Word elaboration mode by a hardwired computational logic (processor comprises a VLIW-RISC engine e.g., see col. 17, lines 62-67) and an additional elaboration channel (channel to element 172,144,174) (or elements 235 or 23) configured to implement plural concurrent data elaboration flows [VLIW processor inherently processing plural instruction flows concurrently].

18. As per claim 16,20 Dye taught that the CPU may comprise a FPGA (e.g., see col. 8,lines 10-13).

***Claim Rejections - 35 USC § 103***

19. Claims 17,18,19,22, 23, 24, 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Dye as applied to claims 15,21 above, and further in view of Dehon.

20. As to claim 17,,22 Dye did not expressly detail that the cell were lookup based cells. DeHon however taught a on chip configurable array comprising lookup based cells (e.g. see fig. 2,2f,5).

21. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Dye and Dehon. . Both references were directed toward the processing of data using signal processing units. One of ordinary skill in the DP art would have been motivated to incorporating the lookup cells teaching Dehon to facilitate programming of the array.

22. As to claim 18, Dehon taught a configurable interconnect (e.g., see fig. 5b).

23. As to claim 19, Dehon taught configuration at the same time as execution (e.g. see col. 21, lines 1-13)[ an therefore the was a requirement for the synchronization of the execution of one portion of the array with configuration of another portion of the array].

24. As per claim 23, DeHon taught transfer to/from registers (e.g., see figs. 2, 2d, 2f). the use of a multiple port register file was within the level of skill in the art of one of ordinary skill in the art.

25. As to claim 24,25, The locking or of a register to prevent a data hazard was well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated in the implementation of the Dye, and DeHon teaching to lock a register when there was a data conflict with a another instruction that required access to the register. Therefore since the data would not have been accessed then the system would

have had to stall processing in the pipeline that was locked out until the data for the competing operation was completed and written back. Clearly this supports highest possible level of resource utilization as it support concurrent execution of instructions as was well known in the art at the time of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



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